Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-27.   (Cancelled)

Claim 28.   (Original)   An integrated circuit comprising:

a shader circuit;

a texture circuit coupled to the shader circuit; and

a frame buffer interface coupled to the texture circuit,

wherein the texture circuit retrieves texture descriptors from a memory.

Claim 29.   (Original)   The integrated circuit of claim 28 wherein the texture circuit retrieves texture descriptors from the external memory using the frame buffer interface.

Claim 30.   (Original)   The integrated circuit of claim 29 wherein the shader provides an instruction for the texture circuit to retrieve the texture descriptors from the graphics memory.

Claim 31.   (Original)   A graphics processor comprising:

a shader circuit;

a texture circuit including a texture cache coupled to the shader circuit; and

a frame buffer interface coupled to the texture circuit,

wherein the texture circuit retrieves a plurality of texture descriptors from an external memory coupled to the frame buffer interface and textures are stored in the texture cache.

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Claim 32. (Original) The graphics processor of claim 31 wherein a base address and index are provided by the shader to the texture circuit for each of the plurality of texture descriptors.

Claim 33. (Currently amended) The ~~method~~ graphics processor of claim 31 wherein an address of a pointer is provided by the shader to the texture circuit for each of the plurality of texture descriptors.

Claim 34. (Currently amended) The ~~method~~ graphics processor of claim 31 wherein an index to a pointer table is provided by the shader to the texture circuit for each of the plurality of texture descriptors.

Claim 35. (Currently amended) The ~~method~~ graphics processor of claim 31 wherein a pointer is provided by the shader to the texture circuit for each of the plurality of texture descriptors.

Claim 36. (Original) An integrated circuit comprising:
a shader circuit;
a texture circuit including a texture cache coupled to the shader circuit; and
a frame buffer interface coupled to the texture circuit,
wherein the shader requests texture descriptors from the frame buffer interface, and the texture descriptors are stored for use by the texture circuit.

Claim 37. (Original) The integrated circuit of claim 36 further comprising:
a texture descriptor cache controller coupled between the shader and the frame buffer interface,
wherein the texture descriptor cache controller receives texture descriptor requests from the shader.

Claim 38.   (New)   The integrated circuit of claim 31 wherein at least one of the plurality of texture descriptors is retrieved a plurality of times.

Claim 39.   (New)   An integrated circuit comprising:

a graphics pipeline;

a shader circuit coupled to the graphics pipeline;

a texture circuit coupled to the shader circuit; and

a frame buffer interface coupled to the texture circuit,

wherein the shader circuit is configured to receive a first texture descriptor, a first hint, and a first command from the graphics pipeline, the first command using the first texture descriptor,

and wherein the texture circuit is configured to receive a second texture descriptor identified by the first hint using the frame buffer interface.

Claim 40.   (New)   The integrated circuit of claim 39 wherein the shader is further configured to receive a first portion of a shader program including a second command and a third command, the second command using the second texture descriptor and the third command using a third texture descriptor,

and wherein the texture circuit is further configured to receive the third texture descriptor using the frame buffer interface.

Claim 41.   (New)   The integrated circuit of claim 40 further comprising:

a first register configured to store the first descriptor;

a second register configured to store the second descriptor; and

a third register configured to store the third descriptor.

Claim 42.   (New)   The integrated circuit of claim 41 wherein the shader is further configured to receive a second portion of a shader program comprising a fourth command, the fourth command using a fourth texture descriptor, and

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wherein the texture circuit is further configured to receive the fourth texture descriptor using the frame buffer interface.

Claim 43.   (New)   The integrated circuit of claim 42 wherein the second register is further configured to store the fourth texture descriptor.

Claim 44.   (New)   ·   An integrated circuit comprising:

a graphics pipeline;

a shader circuit coupled to the graphics pipeline;

a texture circuit coupled to the shader circuit; and

a frame buffer interface coupled to the texture circuit,

wherein the shader circuit is configured to receive a portion of a shader program including a first command, the first command using a first texture descriptor, and

wherein the first texture descriptor is prefetched before the shader executes the first command.

Claim 45.   (New)   The integrated circuit of claim 44 wherein the first texture descriptor is prefetched by the shader circuit.

Claim 46.   (New)   An integrated circuit comprising:

a graphics pipeline;

a shader circuit coupled to the graphics pipeline;

a texture circuit coupled to the shader circuit; and

a frame buffer interface coupled to the texture circuit,

wherein the shader circuit is configured to instruct the frame buffer interface to retrieve a first texture descriptor, and

wherein the texture circuit is configured to receive a first texture from the frame buffer interface, the first texture identified by the first texture descriptor.

Claim 47.   (New)   The integrated circuit of claim 46 wherein the texture circuit comprises:

a texture cache configured to store the first texture.

Claim 48.   (New)   The integrated circuit of claim 47 wherein the texture circuit comprises:

a texture filter configured to filter the first texture.

Claim 49.   (New)   The integrated circuit of claim 46 wherein the shader circuit is configured to retrieve the first texture descriptor a plurality of times.

Claim 50.   (New)   The integrated circuit of claim 46 wherein the texture circuit is configured to receive the first texture a plurality of times.

Claim 51.   (New)   The integrated circuit of claim 46 wherein the first texture descriptor is identified by a base address and index.

Claim 52.   (New)   The integrated circuit of claim 46 wherein the first texture descriptor is identified by an address of a pointer.

Claim 53.   (New)   The integrated circuit of claim 46 wherein the first texture descriptor is identified by an index for a pointer table.

Claim 54.   (New)   The integrated circuit of claim 46 wherein the first texture descriptor is identified by a pointer.